REMARKS

Upon entry of the present amendment claims 1-7 will have been amended to correct informalities in the claim language and to more clearly define the invention, while not substantially affecting or narrowing the scope of these claims and claim 8 has been previously canceled. Applicant respectfully submits that all pending claims are now in condition for allowance.

Applicant notes with appreciation the Examiner's consideration and approval of the drawing corrections filed September 8, 2003.

In the above-referenced Official Action, the Examiner objected to claims 2-7 for minor informalities. Applicant has reviewed these claims and amended the same in order to address the Examiner's concerns. Specifically, "A" has been replaced by --The-- in claims 2-7 and the antecedence has been corrected for the *address-coincidence-disabling system* of claim 2. Thus, it is respectfully asserted that the objection to claims 2-7 has been overcome. Additionally, a minor amendment has been made to claim 1 to correct a misspelling.

Next, the Examiner has rejected claims 1-7 under 35 U.S.C. § 112, first paragraph, asserting that the specification does not reasonably provide enablement for some recitations of claim 1. Applicant respectfully traverses and submits that the specification is sufficiently enabling with respect to the subject matter of claim 1.

Specifically, the Examiner asserts that the *return-address-setter that sets return-address data in the program counter to coincide with the comparison address data* is not enabled by the specification.

One embodiment of the return-address-setter is shown, for example, in Figure 24 and more specifically by logic box 2402, which is part of the process referred to as the "SEQUENTIAL-INTERRUPTION-RETURN-PROCESSING." As described by the first whole paragraph of page 47, the sequential-interruption-return processing can be executed by, inter alia, the control unit 20 (CU) of the CPU 10. Both the CU 20 and the CPU 10 are described on page 15, line 4 et seq. and shown in figure 1, for example only. Next, as described in the specification on page 47, line 21, at step 2402 the return address stored in RAM 14 is set in the program counter 26. When this return address coincides with the comparison address, as described in the first whole paragraph of page 48, the address-coincidence (AC) signal is output from comparator 52 because there is a "coincidence between the return –address and the comparison address." See page 48, lines 5-6 of the specification. The address comparator 52 is shown in figure 2 and described in the specification in the first whole paragraph of page 21.

The Examiner has indicated that the text of page 70, lines 1-15, does not disclose the comparison feature. The disclosure at page 70 is directed to the scrapping feature of the return-address. The one (queried) embodiment of the return-address-setter is fully disclosed in the specification as noted above and page 70 of the specification discloses another aspect of the invention. Thus, it is asserted that the specification provides a full, clear, concise, and exact description of the return-address-setter that sets return-address data in the program counter to coincide with the comparison address.

Next, the Examiner asserts that the *address-coincidence-disabling system that disables the coincidence between the comparison address data and the return-address set in the program counter by said return-address-setter* is not enabled by the specification.

As shown, for example, in Figure 2, the address-coincidence (AC) signal is output from the address comparator 52. If the address-coincidence (AC) signal is not disabled, it is eventually input into the interruption controller 40. The address-coincidence-disabling-system is actuated at least by one of the outputs from ACIPR 58(FD), ACIMR 64(FM), or ACIAR 68(FE) shown in figure 2. The address-coincidence-disabling-system operates in conjunction with any one of the AND gate 54, flip-flop 62, or AND gate 66. Any one of these devices will disable the address-coincidence (AC) signal and not allow it to be input to the interruption controller 40, as shown in figure 2. The ACIPR 58(FD) and its output are described in the specification in the paragraph bridging pages 21 and 22. The ACIMR 64(FM) and its output are described in the specification in the paragraph bridging pages 23 and 24. The ACIAR 68(FE) and its output are described in the specification in the first whole paragraph of page 24.

The Examiner notes in the Official Action that because the disabling system is not adequately disclosed, the objective of the invention at pages 4 and 5 cannot be achieved by the disclosure. However, as noted above, the disclosure provides an adequate and detailed structural and functional description of the *address-coincidence-disabling system.* Thus, it is asserted that the specification provides a full, clear, concise, and exact description of the *address-coincidence-disabling system.*

It thus respectfully asserted that the specification does contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same. Applicants have disclosed examples of specific structure in the specification and the

figures to allow one of ordinary skill to make and use the invention as it relates to the *address-coincidence-disabling system* and *return-address-setter.*

Therefore, Applicant respectfully requests that the Examiner withdraw the rejection under 35 U.S.C. § 112, first paragraph.

It should be further noted that although Applicant has noted particular partitions of the disclosure that provides enablement to the claims under 35 U.S.C. § 112, first paragraph, the claims are not necessarily limited to this particular structure. Applicant notes that these remarks are exemplary of the disclosure, and should not be considered as surrendering equivalents of the territory or a narrowing of the scope of the claims and thus should not be considered a decision by Applicant to narrow the claims in any way.

With regard to claims 2-7, Applicant asserts that they are allowable at least because they depend from independent claim 1, which Applicant submits has been shown to be allowable.

In view of the herein contained amendments and remarks, Applicant respectfully requests reconsideration and withdrawal of previously asserted rejections and objections set forth in the Official Action of October 7, 2003, together with an indication of the allowability of all pending claims, in due course. Such action is respectfully requested and is believed to be appropriate and proper.

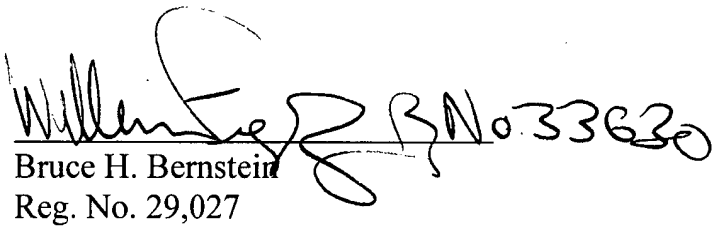
Pursuant to MPEP §714.13, Applicant contends that entry of the present amendment is appropriate because the proposed amended claims avoid the rejections set forth in the last Office Action, resulting in the application being placed in condition for allowance, or, alternatively, the revised claims place the application in better condition for purposes of appeal. Furthermore, the revised claims do not present any new issues

that would require any further consideration and/or search by the Examiner, and the amendment does not present any additional claims without canceling a like number of pending claims. Accordingly, entry of the present amendment is respectfully requested.

Any amendments to the claims which have been made in this amendment, and which have not been specifically noted to overcome a rejection based upon the prior art, should be considered to have been made for a purpose unrelated to patentability, and no estoppel should be deemed to have attached thereto.

Should the Examiner have any questions concerning this Reply or the present application, the Examiner is respectfully requested to contact the undersigned at the telephone number listed below.

Respectfully submitted,
Hiroyuki TAKAHASHI



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